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Design of a High Gain Linear Power Amplifier for 2.4 GHz ISM Band Applications

Firas M. Ali [1]

[1] Department of Electronic Engineering, Faculty of Electrical Engineering, University of Technology, 10066, Baghdad, Iraq.
Email: firas.m.ali@uotechnology.edu.iq

Abstract

High gain linear power amplifiers are needed in modern industrial, scientific, and medical (ISM) systems to increase the transmission range and to produce distortion-free signals. The aim of this paper is to develop a design approach for a multi-stage linear power amplifier that can be used in the 2.4-2.5 GHz ISM band. The amplifier chain consists of three stages to raise the input power level from 0 dBm up to 39 dBm with an overall power gain of 39 dB. The first stage is designed using a medium power GaAs pHEMT transistor by means of the scattering parameters, while the second and third stages are synthesized based on a commercial GaN HEMT power device using the load/source pull technique. Microstrip lines have been used in the implementation of the matching networks to minimize the effects of parasitic elements and to reduce the power losses. The simulation results show an overall DC-to-RF efficiency of 55%, and 38 dBm output RF power at the 1-dB gain compression point (P_{1dB}) across the band of interest. The simulated second harmonic distortion is better than 38 dBc, and the adjacent channel power ratio (ACPR) is high enough at the desired center frequency. These results confirm that the proposed amplifier circuit provides high gain and acceptable efficiency in addition to improved linearity.

Keywords: RF Power Amplifier; GaAs pHEMT; GaN HEMT; ISM Band; ACPR; P_{1dB}.

1 Introduction

Emerged wireless systems require linear amplification of complex-modulated signals to ensure minimum distortion and provide high quality of information. The 2.4 GHz band is widely used in industrial, scientific, and medical (ISM) applications [1]. Linear amplification can be implemented using class-A or class-AB modes at the expense of reduced efficiency. On the other hand, switching mode power amplifiers, like class-E and class-F, can offer improved efficiency but are inherently nonlinear due to active device's ON/OFF operation.

A class-AB medium-power amplifier based on GaAs pHEMT device was proposed to operate at 2.4 GHz [2]. However, the performance metrics indicate low power-added efficiency (PAE) of 12.7% and limited dynamic range. A class E power amplifier has been designed and fabricated with harmonic suppression network to operate at 2.4 GHz [3]. The added harmonic suppression circuit helps to minimize harmonic distortion and improve the efficiency at the expense of increased circuit complexity. A 15W efficient power amplifier was designed and implemented to function in the 2.4-2.5 ISM band with a measured dc-to-RF efficiency of 61% using a harmonic tuning approach [4]. Although the harmonic load impedances are tuned by means of ADS software but this process is difficult to implement practically using extensive load-pull measurements.

A two-stage medium power amplifier was designed based on GaAs pHEMT devices to work at 2.4 GHz [5]. The computer results indicated that an output RF power of 22.5 dBm, power added efficiency (PAE) of 42%, and power gain of 34 dB were obtained at the desired frequency. However, the lumped-element nature of the matching networks restricts the practical implementation of the amplifier to an RF integrated circuit rather than a discrete circuit. A linear amplifier based on microstrip-line matching elements was designed and simulated for operation at the 2.45 GHz ISM band using a GaAs MESFET transistor [6]. The performance characteristics are power-gain of 8.7 dB with output RF power of 19.4 dBm at the 1-dB gain compression point. The main drawback of this amplifier is the limited efficiency and dynamic range due to class-A mode of operation. The linear model of a GaN HEMT device together with a load-line technique was employed in a design process of a 10 W balanced amplifier at 2.4 GHz [7]. This power amplifier

exhibits a drain efficiency of 59% and good linearity. This design approach avoids extensive load-pull measurements and the use of nonlinear CAD transistor models.

The linearity of the class F microwave power amplifier was shown to be enhanced by a developed harmonic control network having a low-pass Chebyshev filtering properties [8]. Based on this modified load network, a medium power microwave amplifier was simulated and implemented using a commercial GaAs pHEMT transistor to provide a power gain of 13.65 dB, output RF power of 23.65 dBm, and a power-added efficiency of 83%.

A fully-integrated two-stage microwave amplifier has been synthesized for operation at 2.4 GHz with output power level of 22 dBm [9]. However, the use of lumped resistors for stability and RF isolation in the matching networks has resulted in low efficiency and significant power dissipation. Finally, an efficient Doherty power amplifier based on Wilkinson power dividers/combiners is synthesized and analyzed [10]. Simulated performance metrics of this amplifier refer to output saturated power of 44 dBm, power gain of 15 dB, and drain efficiency of 95% at 2.4 GHz.

The aim of the current work is to design a high gain and linear power microwave amplifier for the 2.45 GHz ISM band with desired power gain of higher than 35 dB, output RF power of greater than 37 dBm, and overall efficiency of more than 50%.

2 The Proposed Amplifier Block Diagram

The block diagram of the desired power amplifier is constructed from three cascaded stages as illustrated in Figure 1. The first pre-driver amplifier can be designed by means of a small-signal microwave transistor like the GaAs pHEMT AT-34143 of Avago Technologies. This stage is responsible to increase the power level from 0 dBm at the input into about 14 dBm at the output with minimum distortion level. On the other hand, the driver stage is constituted using the GaN HEMT device CGH40006P of Wolfspeed operated as a class-AB power amplifier to raise the signal power from 14 dBm into about 28 dBm. The final stage is a high efficiency power amplifier that utilizes the same CGH4000P device with deep class-AB mode, using very small bias current, to increase the signal level into a saturated output power of 39 dBm approximately.

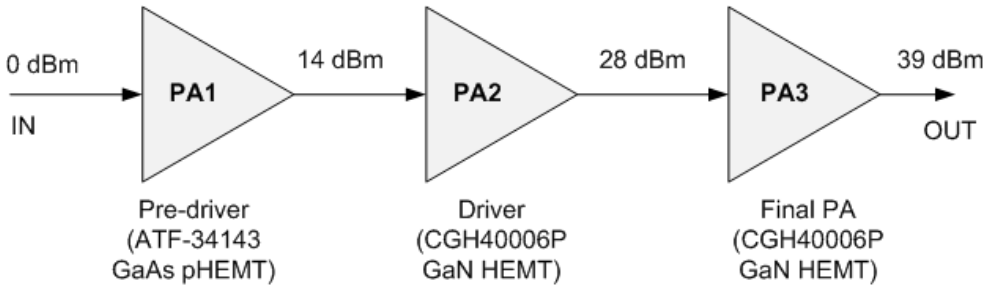

Figure 1: Functional block-diagram of the desired microwave power amplifier.

3 Design of the Pre-driver Amplifier

The first stage of the power amplifier is to be designed by means of the small-signal GaAs pHEMT transistor ATF-34143. The packaged model of this device is first defined to ADS simulator as a sub-circuit. The parasitic package components and die elements are taken from the datasheet. Figure 2 presents the schematic diagram of this transistor which is housed in SOT-323 plastic package with four leads. A DC simulation was carried out for the FET to examine the transfer and output characteristics that are useful in selecting the appropriate *Q*-point. These characteristics are depicted in Figure 3.

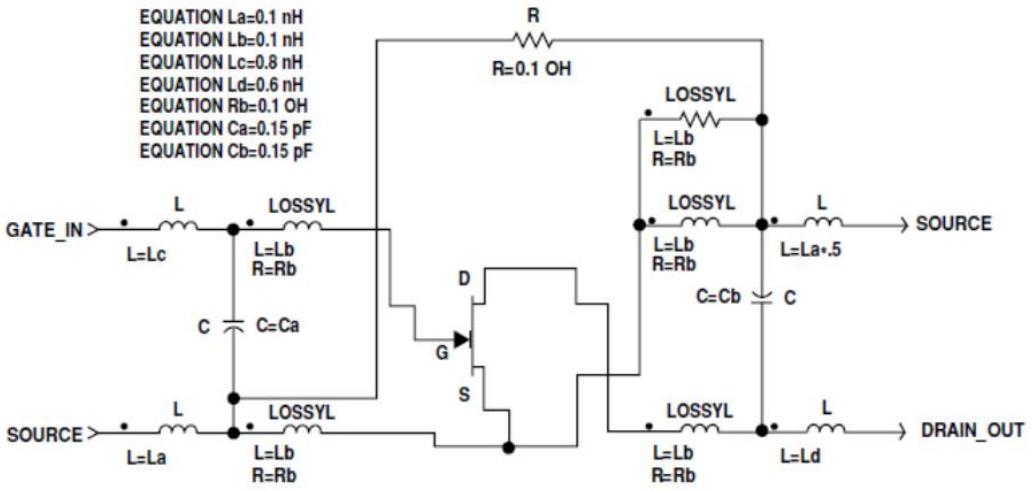

Figure 2: Packaged model of the ATF-34143 GaAs pHEMT.

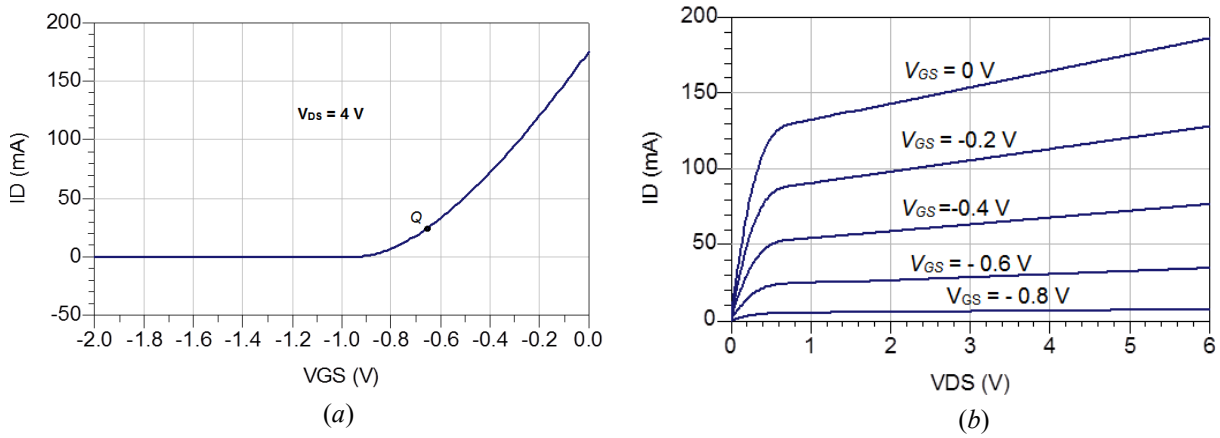

Figure 3: Simulated transfer (*a*) and output (*b*) characteristics of the ATF-34143 GaAs pHEMT.

The selected *Q*-point is set at V_{GSQ} = -0.65 V, I_{DQ} = 25 mA, and V_{DS} = 4 V, where the threshold or pinch-off voltage $V_{GS(th)}$ is equal to -0.9 V approximately. This puts the device in class-AB mode. The scattering parameters of the ATF-34143 device at this *Q*-point was evaluated by means of the ADS S-parameter simulation setup to estimate the maximum available gain and optimum input and output impedances for conjugate matching. It has been shown that the Rollett stability factor (*K*) is lower than 1 for the frequency sweep from 2.4 GHz to 2.6 GHz, and therefore the circuit is potentially unstable. To increase *K* and improve the stability, a series resistance of 8.2 Ω has been inserted at the gate terminal so as to suppress low frequency oscillations [11]. The optimum input and output impedances for maximum achievable power gain of 15.4 dB, after inserting the gate resistor, are Z_{in} = 13.78 – j19.63 Ω and Z_{out} = 25 - j24.7 Ω at 2.5 GHz.

The matching networks at the input and output ports of the amplifier were first synthesized analytically to achieve matching between the optimum transistor terminal impedances and the 50 ohm terminations at a mid-band frequency of 2.5 GHz. Computer optimization was then performed to adjust an optimal response over the band from 2.4 GHz to 2.6 GHz. The circuit schematic of the optimized amplifier is presented in Figure 4.

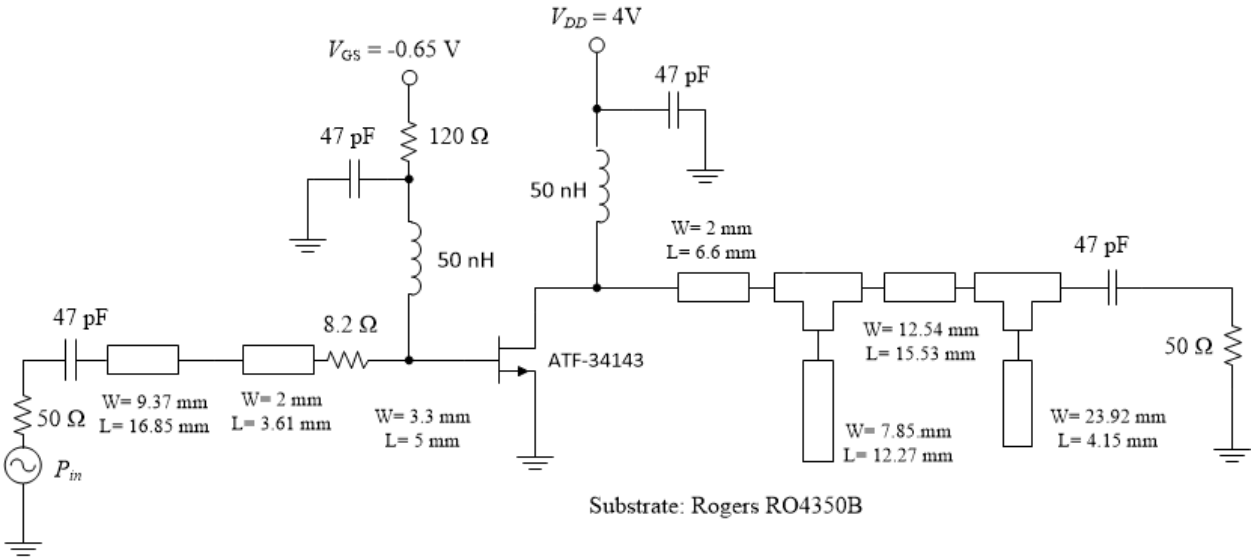

Figure 4: Circuit diagram of the synthesized pre-driver power amplifier.

The matching networks were designed by means of microstrip lines using RO4350B substrate of Rogers with dielectric constant of 3.66, board thickness of 60 mils, copper thickness of 35 µm, and substrate loss-tangent of 0.0032. The input matching network contains two series microstrip-line sections having different widths, while the output matching circuit is constructed by means of two low-pass L-shape sections. Two RF chokes are used for DC feeding to the gate and drain circuits in addition to two blocking capacitors to prevent the DC current from passing into the RF input/output ports. The simulated small signal S-parameters are presented in Figure 5 across a frequency band between 2.4 GHz and 2.6 GHz. The recorded small-signal gain S_{21} is around 15 dB, and the return losses at both the input and output ports are lower than -15 dB, revealing good matching with the 50 Ω terminations and minimum reflected power at both ports. The stability factor is sketched in Figure 6, showing stable operation across this band.

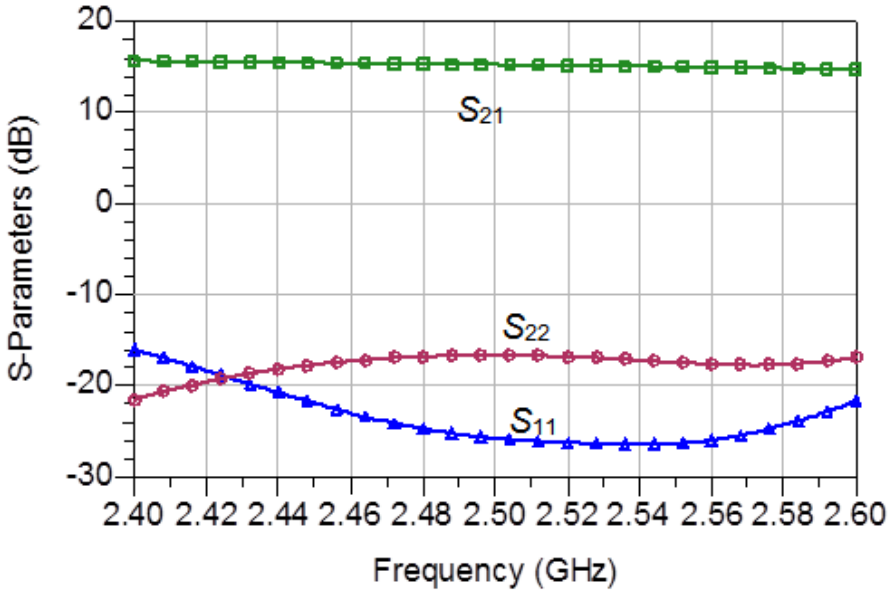

Figure 5: Simulated S-parameters for the pre-driver PA.

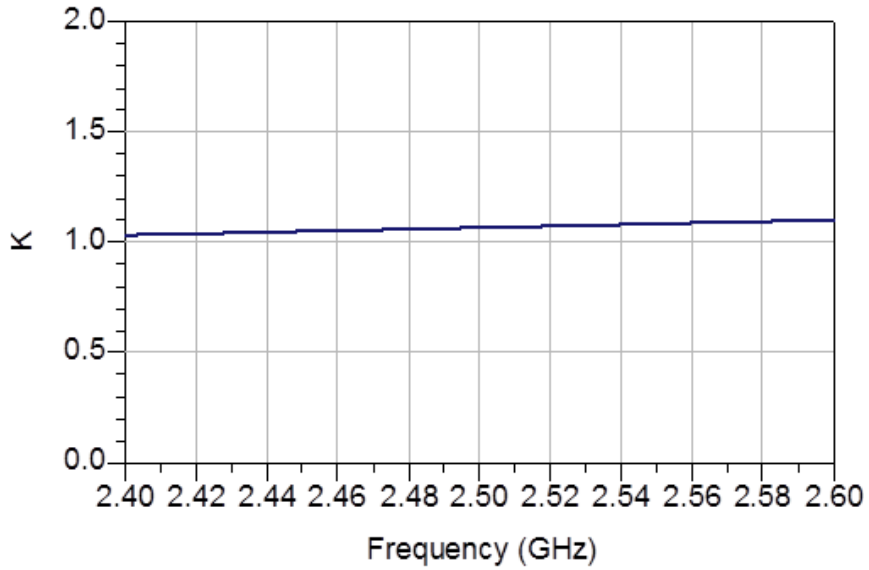

Figure 6: Stability factor versus frequency.

Although the small-signal power gain is about 15 dB, we note that the large signal gain drops with input signal power and is being compressed to about 14 dB at input power level of 0 dBm due to nonlinear operation at large signals. The power output is about 14 dBm at the nominated input signal level. The large signal gain together with the output RF power are sketched against input power (P_{in}) at 2.5 GHz as depicted in Figure 7 using the harmonic balance simulator in ADS.

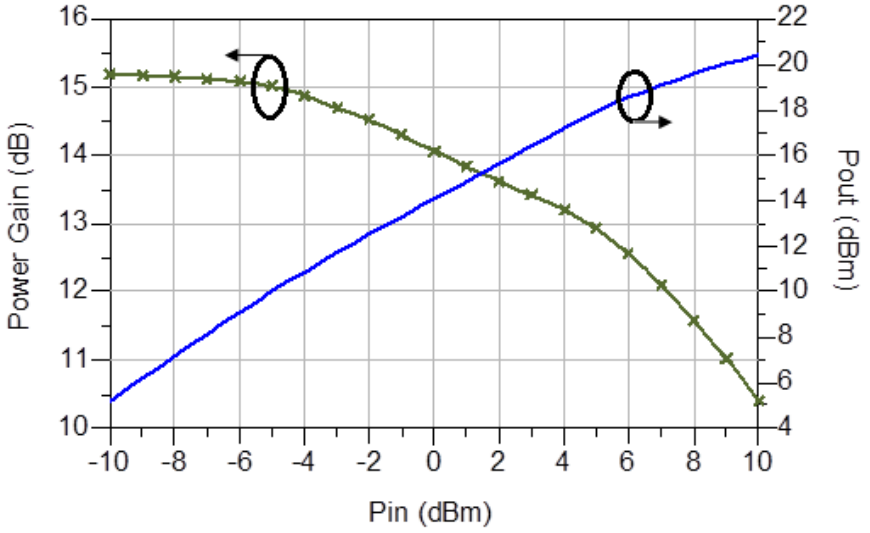

Figure 7: Large signal gain and output RF power against input power level at 2.5 GHz.

4 Design of the Driver Stage

The driver stage is actually a medium power amplifier that should provide an output power of about 28 dBm to the final stage. The GaN HEMT device CGH40006P of Wolfspeed was selected for this amplifier due to its high gain and efficient operation at the S-band frequency range. The transfer characteristic of the power HEMT is simulated and sketched in Figure 8 below. The selected *Q*-point is set at V_{GSQ} = -2.7 V with a drain bias current of 100 mA at drain-to-source voltage of 28 V. In this case, the transistor is biased in class-AB mode. The bias network of the GaN HEMT transistor is quiet simple and consists of gate and drain bias supplies that are isolated from the RF circuit via radio

frequency chokes. An additional current limiting resistor is also inserted in series with the gate choke to prevent any resonant loop at low frequencies and improve circuit stability.

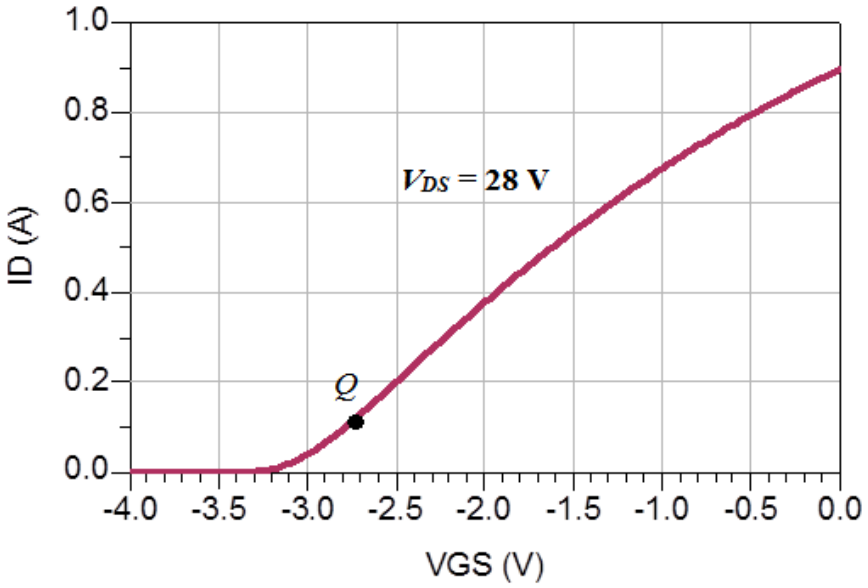

Figure 8: I_D versus V_{GS} for the CGH40006P GaN HEMT.

The optimum large signal input and output impedances for maximum output power were taken from the datasheet of the device at the specified drain bias current and frequency. The designed matching networks are presented schematically in Figure 9. Microstrip line discontinuities like step and cross junctions are used to model the microstrip matching networks. An *RC* network is inserted in the gate circuit to improve the amplifier's stability [11]. The simulation process of the amplifier is carried out with the aid of the harmonic-balance algorithm for non-linear circuits that is equipped with the ADS CAD package. The output RF power and large signal gain are displayed in Figure 10 versus frequency with input power level of 14 dBm.

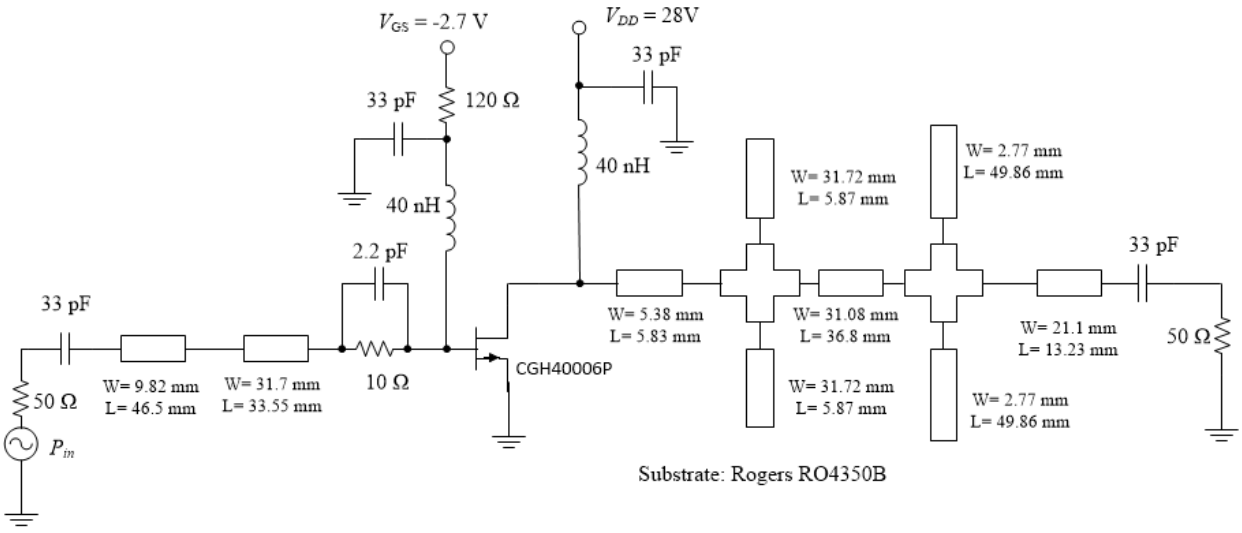

Figure 9: Circuit configuration of the driver power amplifier.

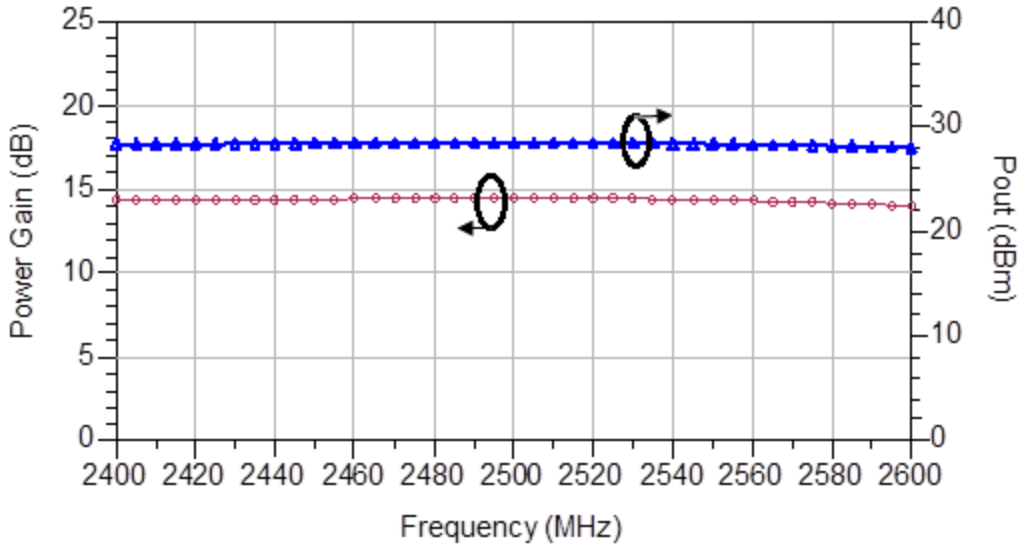

Figure 10: A sketch of power gain and output power versus frequency for the driver stage.

As shown from the sketch in Figure 10, the amplifier can deliver an RF power at the output of 28 dBm with approximate power-gain of 14 dB.

5 Design of the Final Stage

The third stage in the amplifier chain is responsible to deliver the required saturated RF power efficiently into the load. The same HEMT device CGH40006P was selected but with a lower quiescent current to realize deep class-AB (or class-B) mode for higher efficiency. Therefore, a gate-to-source voltage V_{GS} = -3 V was chosen for a drain bias current of 2 mA. The optimum load and source impedances were evaluated by means of the well-known load/source pull test that is equipped with ADS [12]. These impedances represent the optimum terminations for maximized power-added efficiency at the desired frequency and input RF power. The resulting circuit diagram of the third-stage RF power amplifier is shown in Figure 11.

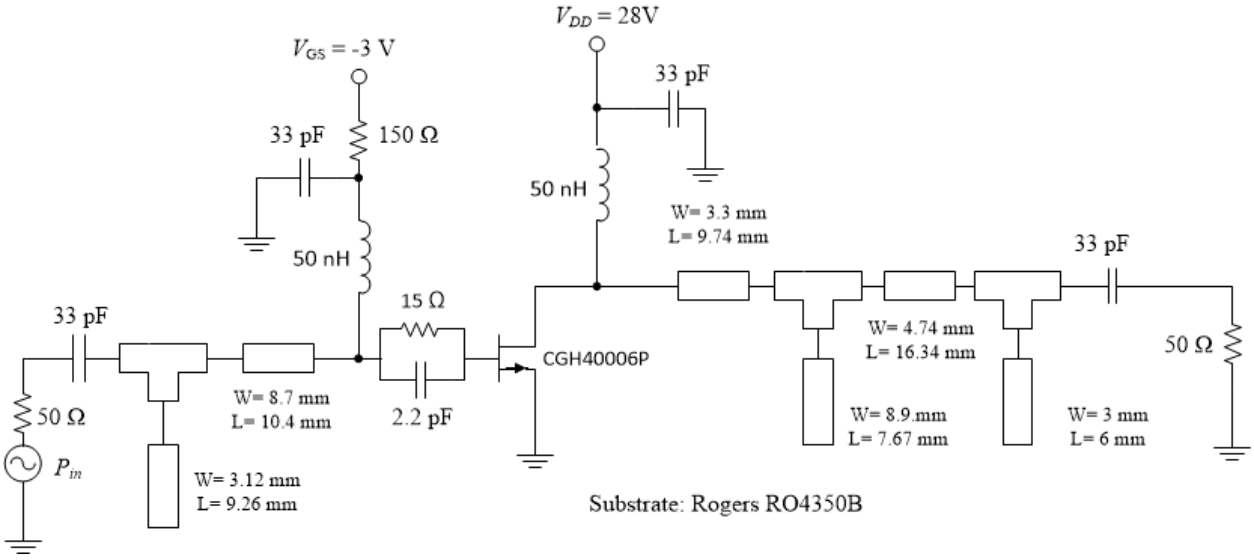

Figure 11: The structure of the final-stage microwave power amplifier circuit.

The input matching network is constituted from a single low-pass L-shape section, while the load network contains two sections to achieve better harmonic suppression at the output. A shunt *RC* circuit is utilized at the gate port of the device to suppress the low frequency oscillations. The input matching network is synthesized for maximizing the power gain and reducing the reflected power at the amplifier's input, while the output matching circuit is constructed for maximized drain efficiency and output signal power.

The simulated large signal gain versus driving power (P_{in}) is presented in Figure 12 for an operating center frequency of 2.5 GHz. The power gain drops abruptly beyond input signal level of 25 dBm, reaching to about 11 dB when P_{in} = 28 dBm. Similarly, the output RF power and DC-to-RF efficiency are displayed in Figure 13. The drain efficiency reaches to about 77.5 % and the output RF power is about 39 dBm at input power level of 28 dBm. The same performance parameters are sketched versus frequency in Figure 14 for an input RF power of 28 dBm and a frequency sweep between 2.4 GHz and 2.6 GHz. It can be seen that a flat response is obtained across the entire band. The drain efficiency is deviating between 74% and 77.5% over the desired band, while the power gain is changing between 10.4 and 10.7 dB.

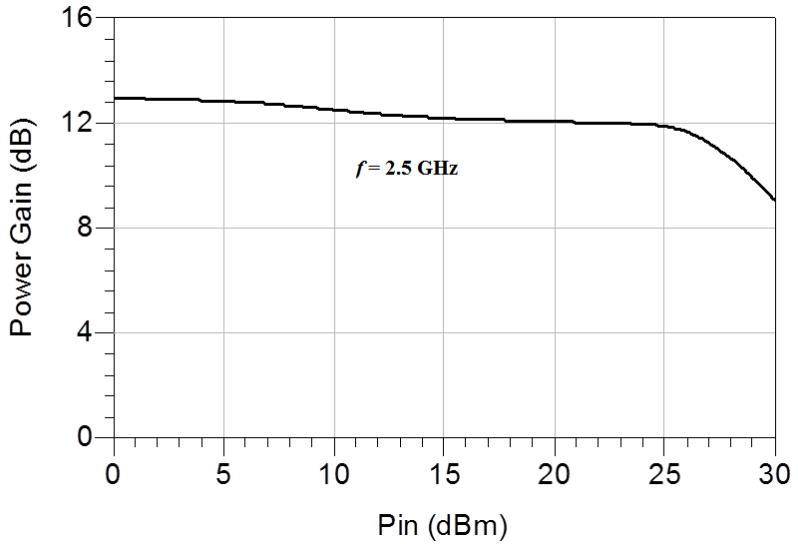

Figure 12: Large signal power gain versus input drive level for the final-stage amplifier at 2.5 GHz.

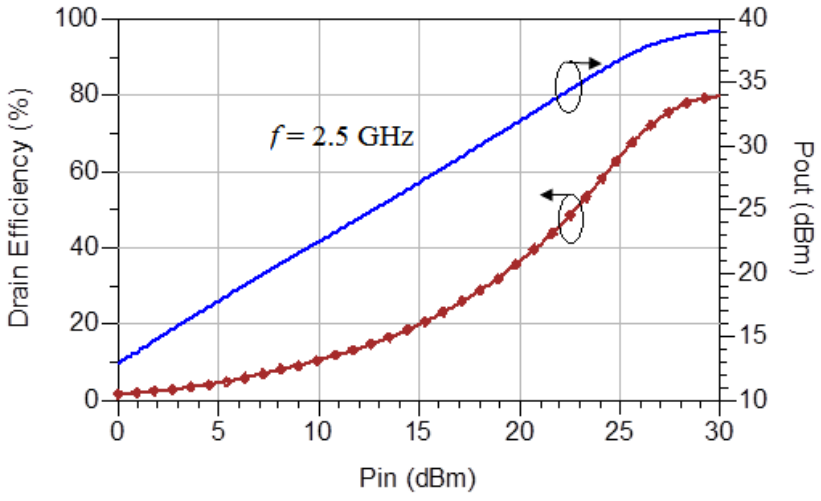

Figure 13: Output power and drain efficiency of the third-stage amplifier against input power at 2.5 GHz.

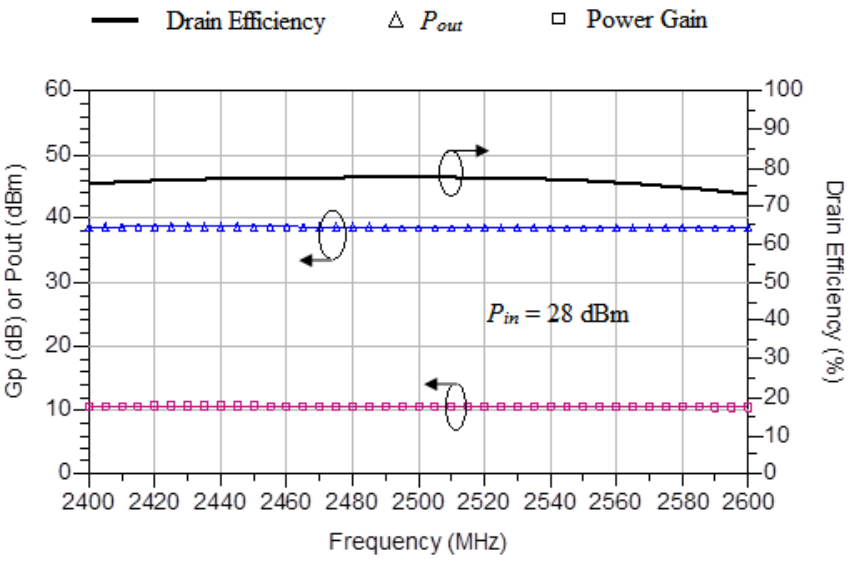

Figure 14: Final stage performance parameters versus frequency.

6 Performance Parameters of the Overall Power Amplifier

The three stages designed thus far are capacitively coupled with each other to constitute the required power amplifier chain. Since all stages are designed for 50 Ω matching, minimum reflected power are expected between the inter-stages.

The total power gain and the output power versus frequency are displayed in Figure 15 for drive power of 0 dBm, showing a flat gain of 39 dB and saturated output RF power of 39 dBm approximately. The overall drain efficiency is calculated from:

$$\eta_D = \frac{P_{out}}{P_{dc1} + P_{dc2} + P_{dc3}} \times 100\% \tag{1}$$

where P_{dc1}, P_{dc2}, and P_{dc3} are the supplied DC power for each individual stage, and P_{out} is the total RF output power.

It is clear from Figure 16 that the simulated drain efficiency is larger than 55%.

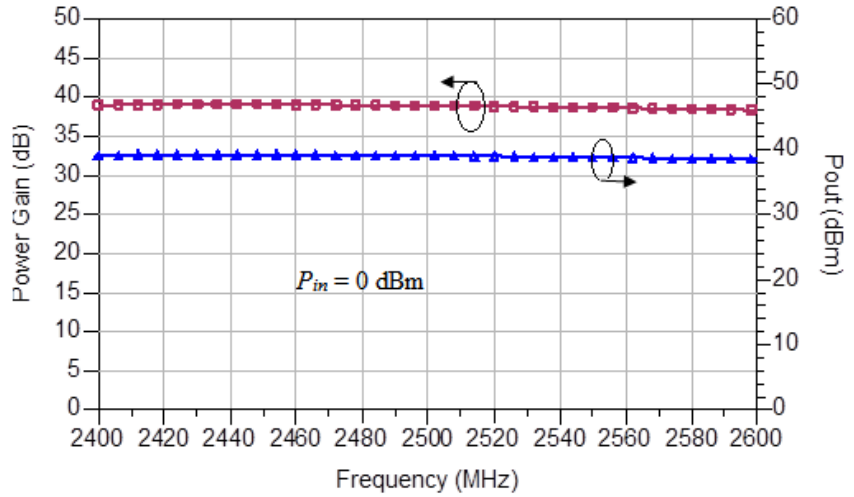

Figure 15: Output RF power and power gain versus frequency for the overall power amplifier.

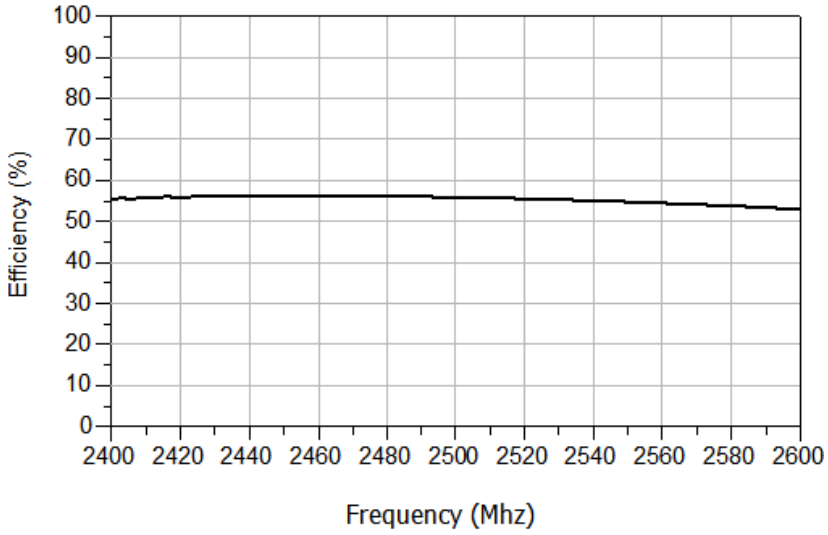

Figure 16: Simulated drain efficiency versus frequency.

The same performance parameters of the combined power amplifier are simulated in Figure 17 versus input RF power with an excitation from -10 dBm to 10 dBm at a frequency of 2.5 GHz. The small signal gain is equal to 42 dB and drops to about 39 dB for a nominated input power of 0 dBm. In other words, the normal large-signal power gain is compressed by about 3 dB from the small-signal linear gain when P_{in} = 0 dBm due to the non-linearity of the power amplifier. It is also clear that the 1-dB gain compression point is satisfied when the driving power P_{in} = -3 dBm, at which P_{out} = 38 dBm.

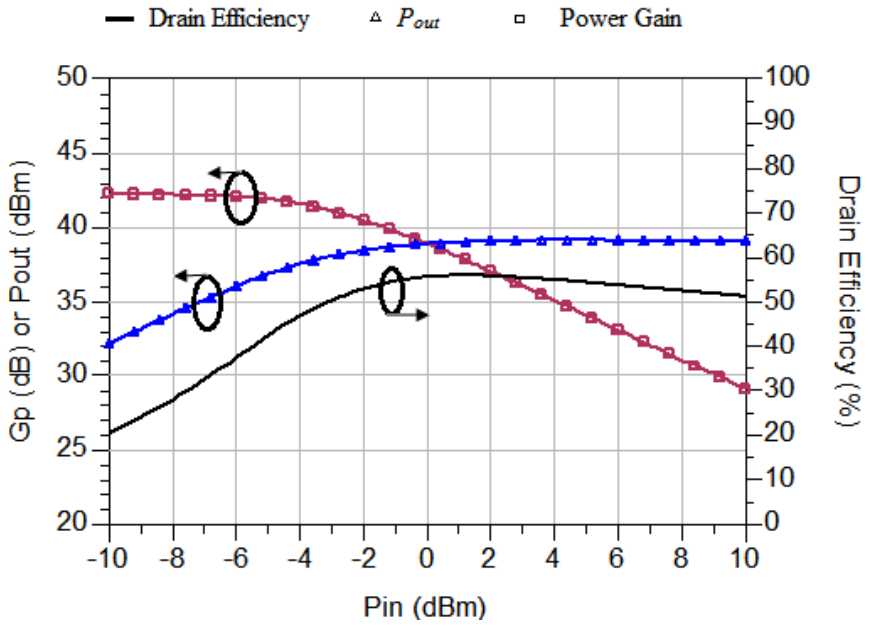

Figure 17: Overall power gain, efficiency, and output RF power against input power at 2.5 GHz.

The power amplifier's linearity is tested by measuring the second harmonic power level relative to the fundamental signal across the entire band, which is sketched in Figure 18. The second-harmonic signal level is less than -38 dBc in this band, indicating an acceptable degree of linearity. The low-pass topology of the matching networks has a major role in reducing the harmonic components in the output signal. Higher order harmonic components are lower than the second harmonic signal level and are ignored in this analysis.

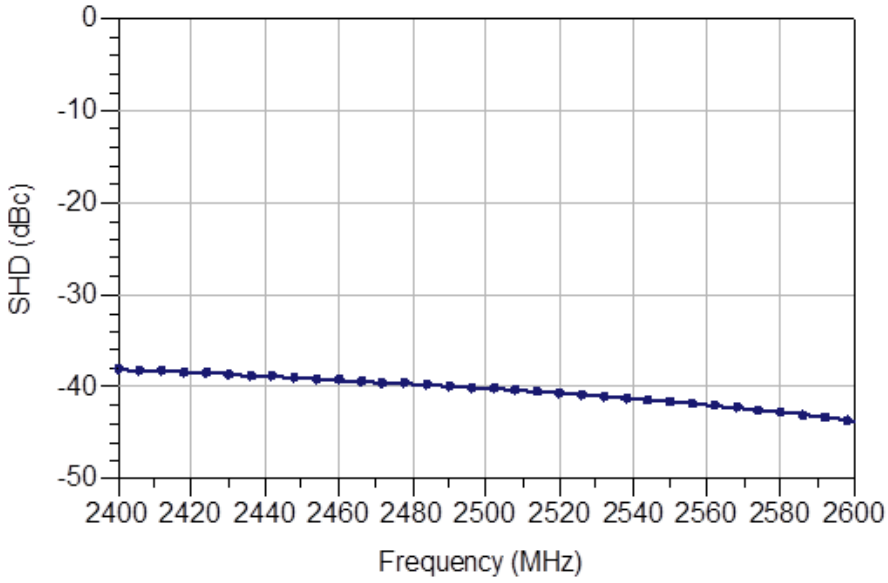

Figure 18: Second harmonic distortion level versus frequency.

A dual-tone source signal is delivered to the input port of the power amplifier with frequencies of 2449 MHz and 2501 MHz, and power level of 0 dBm as demonstrated in Figure 19 to measure the intermodulation distortion (IMD) components. The output signal spectrum is sketched in Figure 20 with a maximum IMD product order of 7. As shown from the sketch, the third order product components are lower than the fundamental component by about 15 dB.

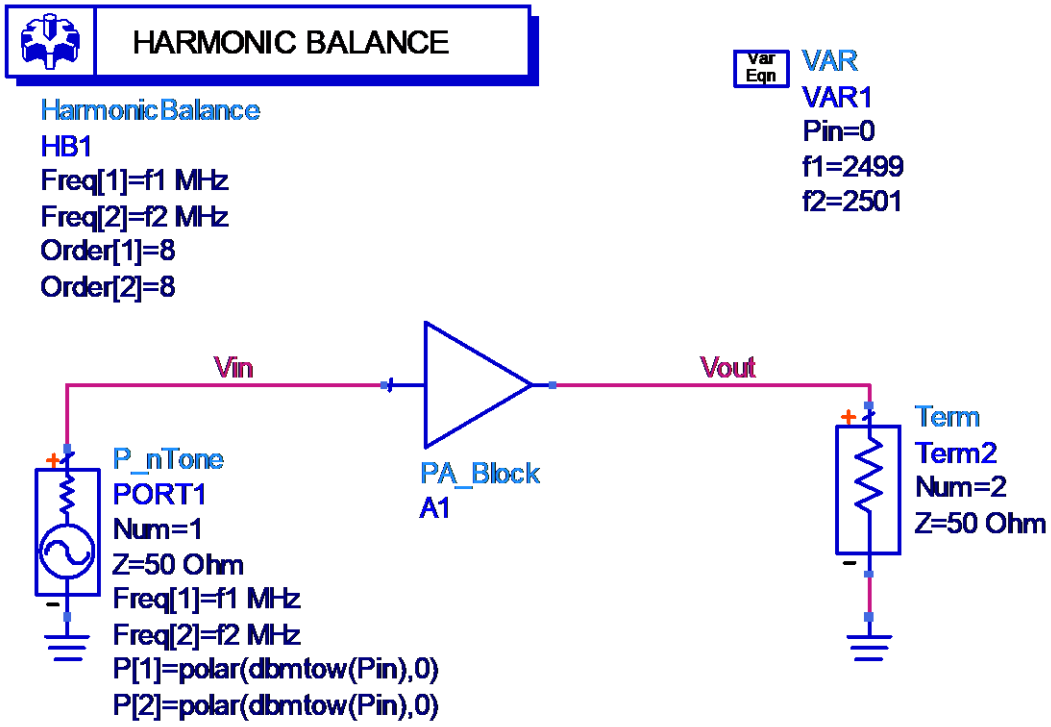

Figure 19: Two-tone test setup.

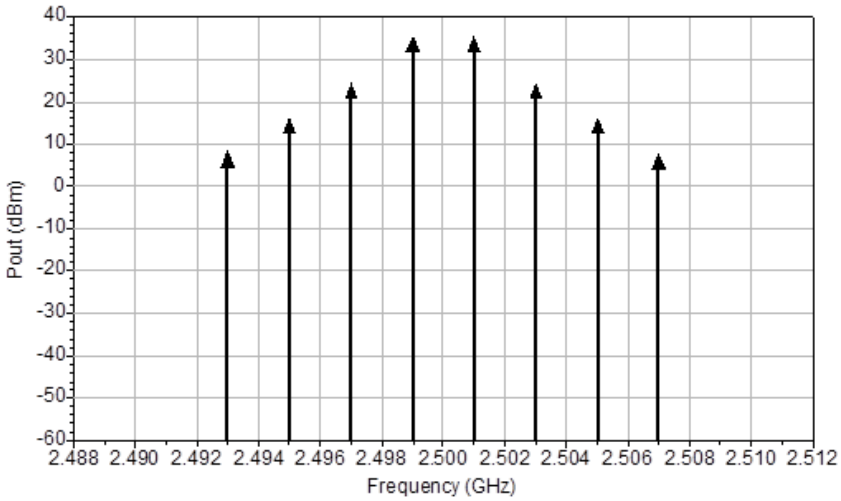

Figure 20: Spectrum of the output signal showing the IMD products.

The recorded results described above represent the ADS computer simulated response. If the amplifier circuit is to be implemented practically then parasitic effects, fabrication imperfections, component tolerances, and fringing field losses may arise and cause some loss in power gain and reduction in output power.

7 Amplifier Response to Modulated Signals

Complex modulated signals like Gaussian MSK, CDMA, QAM, and OFDM are widely used in contemporary wireless communication systems [13]. Some of these modulated signals have constant envelope and do not require a linear power amplifier. Others have variable envelope, where the peak-to-average power ratio is relatively high and therefore require highly linear amplifiers. The linear operation of the power amplifier circuit may be enhanced by some linearization techniques like feedforward, predistortion, and feedback [14].

To investigate the effect of the amplifier non-linearity on a constant envelope signal, a GSM signal is excited to the amplifier with a carrier frequency of 2500 MHz and channel bandwidth of 270 kHz as shown in Figure 21. In this case, the envelope simulation is used instead of the harmonic balance algorithm.

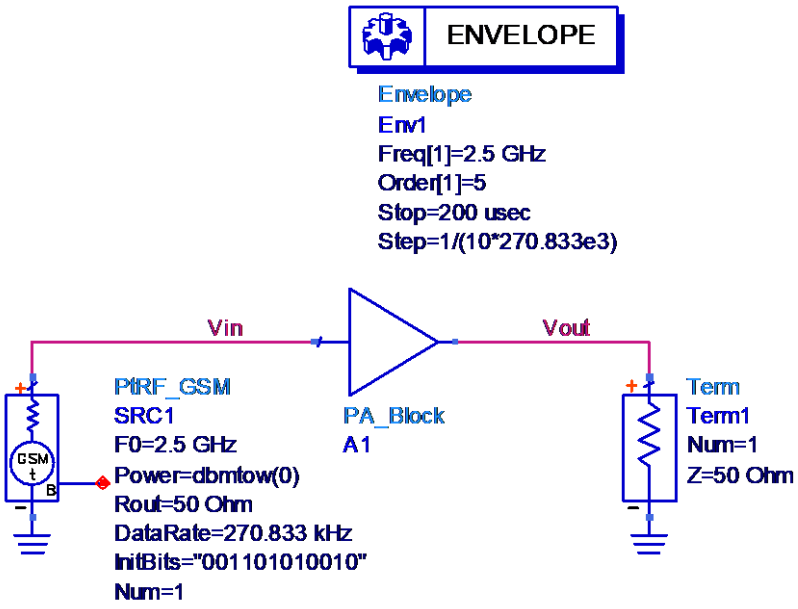

Figure 21: Amplifier simulation setup for a GSM signal.

Figure 22 presents the spectrum of the amplifier's input and output GSM signals. The output signal seems to be an amplified replica of the driving signal with minimal distortion. However, the noise floor is raised and the adjacent channel power ratio, ACPR, is slightly reduced from 85 dBc to 80 dBc approximately. This type of nonlinearity is known as spectral regrowth [14].

Finally, the response of the power amplifier to a wideband CDMA signal is sketched in Figure 23 versus offset frequency. The modulated signal has a carrier frequency of 2.5 GHz and baseband bandwidth of 1.25 MHz. As shown from the plot, the output signal spectrum has a reduced ACPR of 20 dBc when compared with that of the input signal which is about 30 dBc.

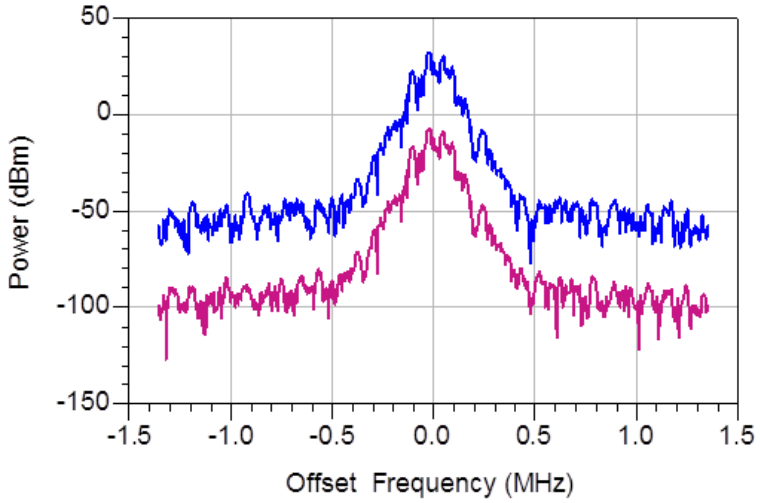

Figure 22: Spectrum of the GSM signals at the input and output terminals of the overall amplifier.

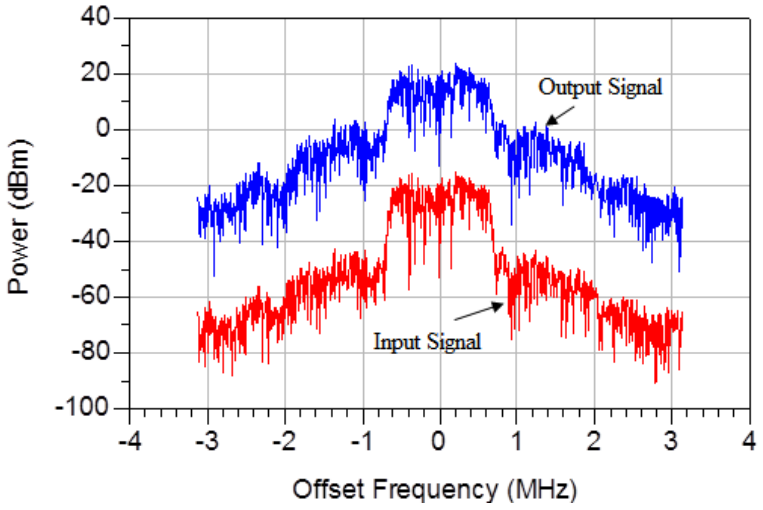

Figure 23: WCDMA signal spectra at the input and output terminals of the overall amplifier.

Although GaN HEMT devices offer efficient and broadband operation, but the high power density of these types of transistors may cause temperature rise due to increased thermal resistance. The thermal effects of these devices can be mitigated practically by using proper heat sinks with materials attaining high thermal conductivity.

8 Conclusion

This article has presented a design technique for a three-stage power amplifier module to operate in the 2.4 – 2.5 GHz ISM band, for applications like the Wi-Fi and Bluetooth standards. The amplifier performance characteristics involve a power gain of 39 dB, conversion efficiency of 55%, and output saturated power of 39 dBm. The circuit was shown to be unconditionally stable at the specified frequency range and input power level. Modern HEMT transistors were

used in the construction of the individual stages with their CAD models to ensure efficient and broadband operation at the desired frequency band. The amplifier linearity was also tested and its response to typical modern wireless signals was verified. Microstrip lines were utilized in the construction of the matching networks using a commercial high quality substrate. The matching circuits are useful in both presenting the proper large signal impedances at the transistors' input/output ports and to suppress the generated harmonics due to their low-pass filter structure. The gathered results indicated that the designed amplifier can significantly boost the transmitted power and compensate the signal losses in long-range faded wireless systems. It can also improve the signal integrity and quality by minimizing the non-linear harmonic distortion and the inter-modulation distortion (IMD). This makes the amplifier circuit suitable for future practical implementation. Future work may also include the enhancement of the amplifier's efficiency using advanced circuit configurations like the Doherty, outphasing, and envelope-tracking techniques that are suitable for modern variable envelope complex-modulated signals.

Funding

This research received no external funding.

Author contribution

A new design approach for a high gain linear power amplifier has been presented and confirmed. A three-stage power amplifier circuit is designed and simulated to operate at the 2.4 GHz industrial, scientific, and medical (ISM) band. It was shown that the designed circuit can give high gain, high output power, good efficiency, and enhanced linearity at the same time in conjunction with the strict requirements of modern wireless applications.

Conflict of interests

The author declares no conflicts of interest.

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